	L #	Hits	Search Text	DBs	Time Stamp
1	L1	25	duration near2 "programming cycle"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/15 13:19
2	L2	7	1 and test	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/15 13:21
3	L3	7	2 and flash	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/15 13:28

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	1	3 and (gate near (insulator or insulating))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/15 13:28
5	L5	0	("2005/0009217").URPN.	USPAT	2005/06/15 13:28
6	L6	1	3 and ("SiO.sub.2" or SiN or "silicon dioxide" or "silicon nitride")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/15 13:29

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TITLE: Parallel programming of multiple-bit-per-cell memory
cells on a continuous word line

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Abstract Text - ABTX (1):
Write operations that simultaneously program multiple memory cells on the same word line in an MBPC **Flash** memory employ word line voltage variation, programming pulse width variation, and data-dependent bit line and/or source line biasing to achieve uniform programming accuracy across a range of target threshold voltages. A first type of write operations reaches different target threshold voltages during different time intervals, but uses word line signals that optimize threshold voltage resolution regardless of the target threshold voltage. A second type uses bit line and/or source line biases that depend on the multi-bit data values being written so that different memory cells reach different target threshold voltage at about the same time. Source line biasing can also reduce bit line leakage current through unselected memory cells during read or verify operations. A memory includes divided source lines that permit separate data-dependent source biasing. During or at the end of write operations, remedial programming sequences can adjust the threshold voltages of memory cells that program slowly.

Brief Summary Text - BSTX (2):
Many memory manufacturers are developing multiple-bit-per-cell (MBPC) memories to increase storage density and lower memory cost. MBPC **Flash** memories, for example, have greater storage density than do binary memories

and
source voltages on the relation between the threshold voltage and accumulated
programming time for a **Flash** memory cell.

Drawing Description Text - DRTX (15):
FIG. 11 shows a MBPC **Flash** memory having a divided source line that permits
data-dependent source line biasing during a write operation.

Drawing Description Text - DRTX (16):
FIG. 12A shows a layout for continuous source lines for a conventional **Flash**
memory.

Drawing Description Text - DRTX (17):
FIG. 12B shows a layout for divided source lines for a **Flash** memory in
accordance with an embodiment of the invention using data-dependent source
biasing.

Drawing Description Text - DRTX (18):
FIG. 13 shows a MBPC **Flash** memory employing data-dependent source line
biasing and data-dependent programming loads during a write operation and
having split bit lines.

Detailed Description Text - DETX (3):
In accordance with an aspect of the invention, a MBPC **Flash** memory having
continuous word lines implements write operations that set multiple threshold
voltages when simultaneously programming multiple memory cells that are
connected to the same word line. In one embodiment of the invention, a write
operation reaches different target threshold voltages near the ends of
corresponding time intervals, and the programming voltages and/or the **duration
of programming cycles** during the write operation change to provide uniform
threshold voltage resolution for the target threshold voltages. In another
embodiment of the invention, memory cells being programmed have drain and/or
source biasing that depend on the target threshold voltages for the memory

speed, and the capabilities of high voltage charge pumps in the memory. For uniform programming accuracy across the range of target threshold voltages, the programming voltage change .DELTA.Vpp per programming cycle 316 is ideally selected so that each programming cycle 316 causes the same threshold voltage step .DELTA.Vt in a memory cell being programmed. A programming voltage change .DELTA.Vpp per programming cycle 316 can be, for example, about equal to the desired threshold voltage step .DELTA.Vt per programming cycle. However, small uniform threshold voltage steps .DELTA.Vt require more programming cycles 316, and the number of programming cycles 316 needed to reach the maximum word line programming voltage Vpphi determines the write speed. For example, to achieve a threshold voltage resolution smaller than 100 mV, the programming voltage change .DELTA.Vpp will be about 100 mV or less, and more than 30 or more programming cycles 316 (and 30 or more verify cycles 320) would be required to reach maximum programming voltage Vpphi of 10 V if the starting programming voltage Vpplo is 7 V. If the programming voltage change .DELTA.Vpp were increased to 200 mV, the write operation would require half as many programming and verify cycles, but the threshold voltage resolution would be poorer because of the resulting corresponding increase in the threshold voltage change .DELTA.Vt per programming cycle. The write operation of FIG. 3B with a staircase-increasing word line voltage and uniform **duration programming cycles** thus requires tradeoffs between write speed and threshold voltage resolution.

Detailed Description Text - DETX (30):

FIG. 5C illustrates timing diagrams for a write operation similar to that of FIG. 5B, but the write operation of FIG. 5C uses **programming cycles of varying duration**. In particular, to improve the precision of threshold voltage

resulting from the write operation of FIG. 5C, the **duration of programming cycles** 510-0 near the end of interval I0 are shorter than the **duration of programming cycles** 510-0 at the start of interval I0. The shorter programming cycles cause less threshold voltage change per programming cycle 510-0, so that the results of a verify cycle stops further programming cycles when the memory cell is near to target threshold voltage Vt0. After the end of interval I0, the length of programming cycles 510-1 in the next interval I1 return to the longer duration.

Detailed Description Text - DETX (33):

The method of varying the **duration of programming cycles** during each interval is also subject to variation. FIG. 5C illustrates a case where programming cycles continuously decrease in duration until the end of each interval I0, I1, I2, and I3 and then transition back to the longer duration at the start of the next interval. One alternative method uses only two different lengths for the **duration of programming cycles**. The longer of the two programming cycles is used at the start of each of the intervals I0, I1, I2, and I3 for faster programming, but during each interval, the programming cycles switch to the shorter length when a characterization of the memory cells indicates that fast programming memory cells may be reaching the target threshold voltage corresponding to the interval.

Detailed Description Text - DETX (41):

FIG. 7A contains plots 730, 735, 740, and 745 showing the variation of the threshold voltage of a typical **Flash** memory cell with accumulated programming for applied drain voltages Vd of 3.0, 3.5, 4.0, and 4.5 volts, respectively. A gate voltage Vg of 10 volts and a source voltage Vs of 0 volts apply to each of plots 730, 735, 740, and 745.

Detailed Description Text - DETX (42):

Multi-bit-data-dependent biasing can also be implemented on the source side of selected memory cells if the MBPC memory contains appropriate source line architecture, decoders, and drivers. FIG. 7B contains plots 702, 707, 712, and 717 showing the variation of the threshold voltage of a typical **Flash** memory cell with accumulated programming for applied source voltages Vs of 0.25, 0.75, 1.25, and 1.75 volts, respectively. A gate voltage Vg of 10 volts and a drain voltage Vs of 4.5 volts apply to each of plots 702, 707, 712, and 717.

Detailed Description Text - DETX (50):

FIG. 8D shows timing diagrams for yet another write operation in accordance with the invention. The write operation employs both variable word line programming voltages and variable **duration for programming cycles** 810D. In particular, programming cycles 810D at the start of the write operation use the minimum word line programming voltage Vppmin to limit the programming currents that charge pumps must supply when memory cells have low threshold voltages. Further, to reduce the time spent on verify cycles when the selected memory cells are likely to be far from their respective target threshold voltages, initial programming cycles 810D have the longest duration. The word line programming voltage increases and the **duration of programming cycles** 810D decrease as the threshold voltages of the memory cells increase and near their respective target threshold voltages until programming cycles 810D reach a minimum duration and/or a maximum word line programming voltage Vppmax. The word line programming voltages used during programming cycle 810D increases in voltage steps that can either be uniform or non-uniform as discussed with reference to FIGS. 3B and 5A.

Detailed Description Text - DETX (51):

FIG. 8E illustrates another embodiment of a write operation using both variable word line programming voltages and variable **programming cycle duration** with multi-bit data-dependent bit and/or source line biasing. The write operation of FIG. 8E differs from the write operation of FIG. 8D in that the **duration of programming cycles** increases throughout the write operation of FIG. 8E. Increasing the **duration of the programming cycles** 810E can compensate for the smaller rate of threshold voltage change when the threshold voltage of a memory cell is high relative to the available word line programming voltage. FIG. 8E also illustrates a word line programming voltage that increases non-uniformly from one programming cycle 810E to the next.

Detailed Description Text - DETX (57):

In each of the intervals, I0, I1, I2, and I3 of FIG. 9A, the **duration of respective programming cycles** 910-0, 910-1, 910-2, and 910-3 are longer at the beginning of the interval and shorter at the end of the interval. The decrease in duration can be done as illustrated in FIG. 9A in a single step from longer **duration programming cycles** when memory cells are expected to be far from their target threshold voltages to shorter **duration programming cycles** when memory cells may be nearing their target threshold voltages. Alternatively, the **duration of programming cycles** can continuously decrease in duration during each interval I0, I1, I2, and I3 or the fixed duration could be used throughout.

Detailed Description Text - DETX (67):

In the embodiment of FIG. 10, remedial programming 1060 includes a first set of programming cycles 1012 that have an increased **duration (e.g., programming cycles** of 300 ns instead of 200 ns) to increase the threshold voltage change per cycle. Increasing the **duration of the programming cycles** generally provides a disproportionately greater increase in the effective

programming cycles have shorter duration at an end of a first interval than at a start of the first interval; increase in duration immediately after the first interval, and for a second interval that follows the first interval have shorter duration at an end of the second interval than at a start of the second interval.

Claims Text - CLTX (12):

12. The write operation of claim 10, wherein during each interval, **programming cycles have longer duration** at the start of the interval than at the end of the interval.

Claims Text - CLTX (14):

14. The write operation of claim 13, wherein the first set of programming parameters includes a first **duration for programming cycles** during which the threshold voltage of the selected memory cell changes, and the second set of programming parameters includes a second **duration for the programming cycles, the second duration** being longer than the first duration.